AMENDMENT

In The Claims:

Please amend the claims as follows.

Claims 1-16 (canceled)

17. (currently amended) A NAND Mask ROM, comprising a plurality of word lines, a plurality of bit lines, and a plurality of memory cells arranged in rows and columns, wherein

the memory cells include a plurality of first memory cells that have a first channel conductivity and are depletion MOS transistors, and a plurality of second memory cells that have a second channel conductivity and are enhanced MOS transistors;

the memory cells in the same row are coupled to a word line, and the memory cells in the same column are coupled to a bit line;

a constant number of continuous memory cells in the same column are grouped as a memory string, wherein

a non-terminal memory cell shares a source and a drain with two adjacent memory cells in the memory string; and

one terminal memory cell in the memory string is coupled to a bit line, and the other terminal memory cell is coupled to ground,

wherein gate electrodes of the memory cells in the same row are coupled to a word line with contacts.

18. (original) The NAND Mask ROM of claim 17, wherein the memory cells comprise NMOS transistors, the first memory cells comprise depletion NMOS transistors that have N-type channels, and the second memory cells comprise enhanced NMOS transistors that have P-type channels.

19. (original) The NAND Mask ROM of claim 17, wherein the memory cells comprise PMOS transistors, the first memory cells comprise depletion PMOS transistors that have P-type channels, and the second memory cells comprise enhanced PMOS transistors that have N-type channels.

Claim 20. (cancelled)

21. (currently amended) ~~The NAND Mask ROM of claim 17,~~ A NAND Mask ROM, comprising a plurality of word lines, a plurality of bit lines, and a plurality of memory cells arranged in rows and columns, wherein

the memory cells include a plurality of first memory cells that have a first channel conductivity and are depletion MOS transistors, and a plurality of second memory cells that have a second channel conductivity and are enhanced MOS transistors;

the memory cells in the same row are coupled to a word line, and the memory cells in the same column are coupled to a bit line;

a constant number of continuous memory cells in the same column are grouped as a memory string, wherein

a non-terminal memory cell shares a source and a drain with two adjacent memory cells in the memory string; and

one terminal memory cell in the memory string is coupled to a bit line, and the other terminal memory cell is coupled to ground,

wherein two memory strings adjacent in the row direction share one bit line, the two adjacent memory strings consisting of a first memory string and a second memory string.

22. (currently amended) The NAND Mask ROM of [[~~claim21~~]]claim 21, wherein

each memory string is selected with a pair of bank select transistors, including a depletion MOS transistor and an enhanced MOS transistor that are coupled, wherein one of the two bank select transistors is coupled to a terminal memory cell in the memory string;

the two pairs of bank select transistors [[~~of the~~]] are arranged in two rows and two columns, wherein two bank select transistors in the same row are coupled to a bank select line with gate electrodes thereof, and two terminal bank select transistors accompanied with the two adjacent memory strings are coupled to the bit line; and

the depletion (or enhanced) MOS transistor among the pair of bank select transistors for selecting the first memory string is coupled to a bank select line together with the enhanced (or depletion) MOS transistor among the pair of bank select transistors for selecting the second memory string.

23. (original) The NAND Mask ROM of claim 22, wherein one of the two bank select transistors for selecting a memory string shares a diffusion with a terminal memory cell in the memory string.

24. (original) The NAND Mask ROM of claim 22, wherein the depletion MOS transistor and the enhanced MOS transistor in a pair of bank select transistors for selecting a memory string share a diffusion.

25. (original) The NAND Mask ROM of claim 22, wherein the two terminal bank select transistors accompanied with the two adjacent memory strings share a diffusion that is coupled to the bit line.

26. (original) The NAND Mask ROM of claim 17, wherein a memory string is coupled to a bit line, and does not share the bit line with another memory string adjacent in the row direction.

27. (original) The NAND Mask ROM of claim 26, wherein one terminal memory cell in a memory string is coupled to a bit line via one bank select transistor.

28. (original) The NAND Mask ROM of claim 17, wherein a diffusion of the other terminal memory cell in the memory string is coupled to a ground line via a contact.

29. (original) The NAND Mask ROM of claim 17, wherein two memory strings are separated by an isolation layer.

30. (original) The NAND Mask ROM of claim 17, wherein the constant number is 8.